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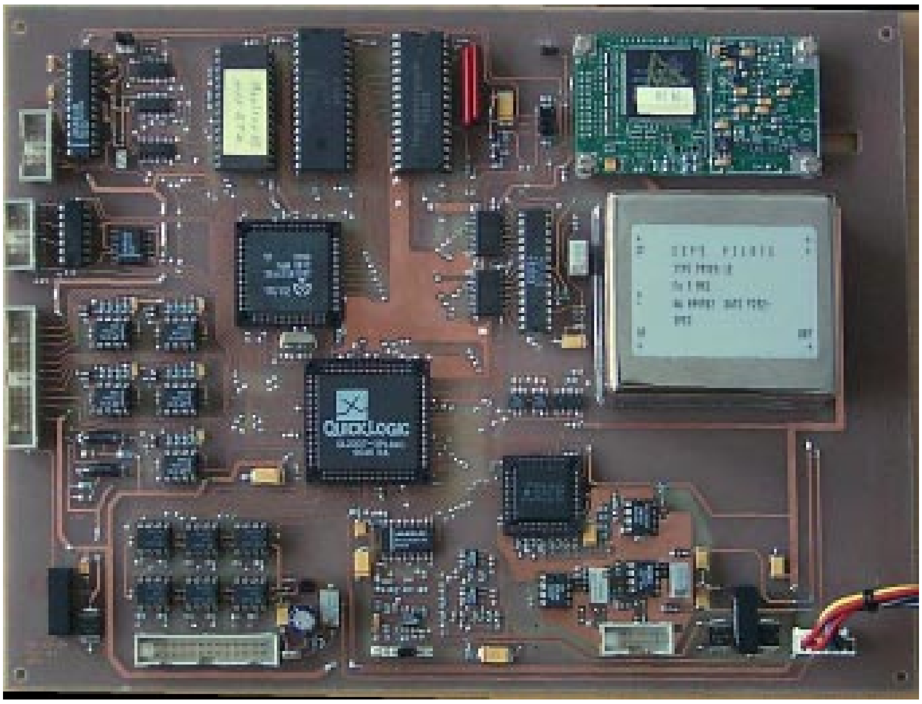
Technical Report

A GPS Based Time Synchroniser

Gunnar Sundin
Åke Arvidsson
Jörgen Pihl
Håkan Lans



Division of Systems and Underwater Technology
SE-172 90 STOCKHOLM

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Gunnar Sundin
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Jörgen Pihl
Håkan Lans

Document title

A GPS Based Time Synchroniser

Abstract

The report describes a GPS synchronised clock. Its intended use is to synchronise transmitter and receiver in a bistatic sonar system. It uses the one-second-pulse form a GPS receiver to synchronise the clock to UTC time and at the same time to steer the built in oscillator to exactly 5 MHz. After the synchronisation the clock is estimated to keep its time to within a few milliseconds for a period of two months. Thus the clock can be used even if the GPS signal is not available for a long time as in a submarine. When the GPS signal is available, the accuracy of the clock is expected to be better than 100 ns. With a built in direct digital synthesis chip the clock can also deliver a sinusoidal signal which can be modulated in amplitude, frequency or phase.

Key words

Synchronised clock, GPS, Bistatic Sonar, Multistatic Sonar, Direct Digital Synthesis

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Dokumentets titel i översättning

En GPS-synkroniserad klocka

Sammanfattning

Rapporten beskriver en GPS-synkroniserad klocka. Den är avsedd att synkronisera sändare och mottagare i ett bistatiskt sonarsystem. Den använder ensekundpulserna från en GPS-mottagare för att synkronsera klockan till UTC-tid och styr på samma gång den inbyggda oscillatorn till exakt 5 MHz. Efter synkroniseringen förväntas klockan hålla tiden inom ett par millisekunder under en tid av två månader. Klockan kan alltså även användas då GPS-signalen inte är tillgänglig under lång tid som i en ubåt. När GPS-signalen är tillgänglig är klockans förväntade noggrannhet bättre än 100 ns. Med ett inbyggt DDS-chip (direct digital synthesis) kan klockan även lämna en sinussignal som kan moduleras i amplitud, frekvens och fas.

Nyckelord

Synkroniserad klocka, GPS, Bistatisk sonar, Multistatisk sonar, Direct Digital Synthesis

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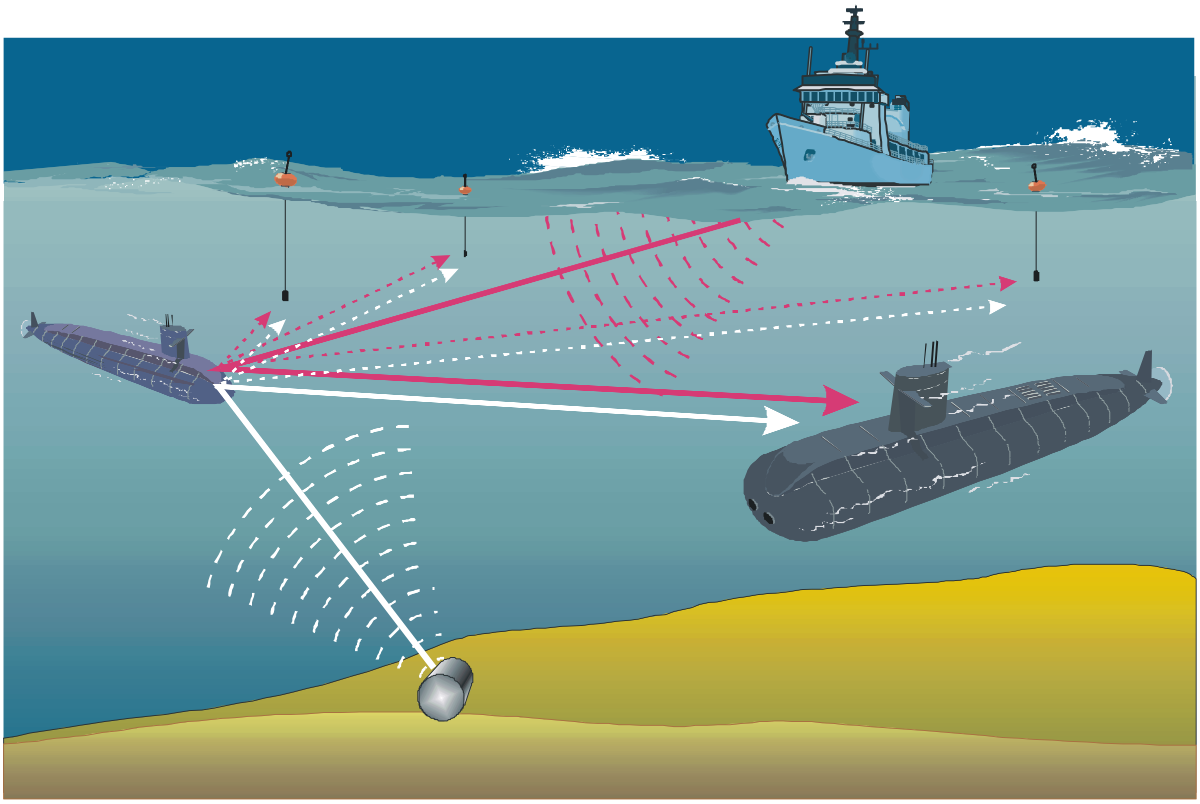


Figure 1. *Examples of Multistatic Sonar in active surveillance. One transmitter is fixed at the bottom, and the other onboard the surface ship. Receivers are positioned at the surface (sonobouys) and onboard the own submarine. The positions of the receivers are unknown to the target submarine.*

1. Introduction

1.1 The Multistatic Sonar

Modern submarines and surface ships are becoming more and more quiet. As a result, the detection distances for passive sonar are getting shorter. A possible way around this problem is to use active sonar, which might give you the detection distances you need. However, using active sonar might be undesirable for a submarine, which wants to operate silently and covertly. By putting the transmitter on a co-operating platform and the receiver on the submarine, it can still be silent but gain from the longer detection distances obtainable by the active sonar. Such a sonar is called a Multistatic Sonar (Figure 1).

Multistatic sonar has been tested by several nations (1). At FOA we are just now setting up a test system to investigate the performance of multistatic sonar in the Baltic. Figure 2 shows a schematic picture of an experimental setup. In this example the transmitter, the target and the receiver are at the corners of a triangle (Tr-T-R). To know the position of the target the receiver has to know the length of the triangle side C and the direction to the target. This can be computed if the distances A and (B+C) are known. Then the target must lie on an ellipse, and if the direction to the target is known its position can be uniquely determined. Thus if the position of the sender and the time of the transmission is known the position of the target can be determined.

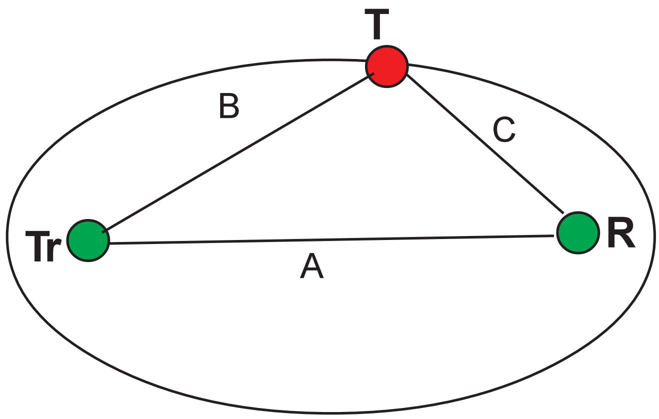


Figure 2. *Principle of Multistatic Sonar*

By using several transmitters, and/or several receivers, we obtain a pattern of overlapping ellipses. In such cases the target position can be determined even if the direction is not known.

1.2 Requirements

In multistatic sonar the receiver must know the time when the transmitter emits a pulse. A radio link or a direct cable connection usually achieves this time synchronisation. However, if the receiver is on a submarine or another submerged platform, we can not establish a communication link. One way in such a case to obtain time synchronisation is to have very accurate clocks at the transmitter and receiver. These clocks need to be accurate enough so that negligable errors are introduced in the signal processing. In principle, the accuracy in timing should be better than the accuracy in positioning and target localisation. The latter depends on the emitted pulse type and length, the processing mode, and the selected range of search. The best obtainable range estimates of a surveillance sonar are of the order of one meter, corresponding to a few milliseconds accuracy in time. The goal of our design is to achieve an accuracy of one millisecond over a period of two months, which corresponds to an estimated maximum time for a submarine operation.

2. Design and operational principles

2.1 Basic ideas behind the GPS synchronisation unit

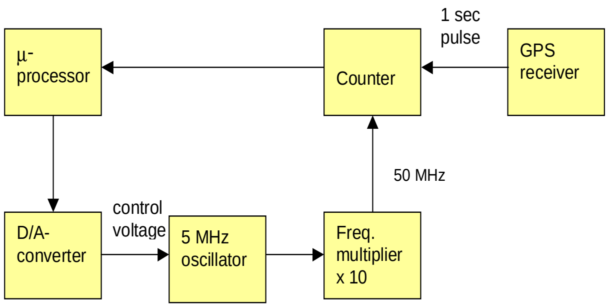
The main components of the time synchronisation unit are a very stable oscillator, a GPS receiver, a microprocessor and a logic unit built into a FPGA circuit.

Figure 3 shows the basic structure of the synchronisation control loop. The frequency of the oscillator can be varied by changing the voltage applied to one of its connections, but only within a small range around 5 MHz. With the frequency multiplier, the accuracy of the control loop is increased tenfold.

A period counter counts the periods of the 50 MHz signal from the frequency multiplier for an integer number of seconds. The microprocessor compares the output from the counter with the corresponding value from a true 50 MHz oscillator. If a difference is observed, it sends a command to the D/A converter to change the frequency of the oscillator to make it closer to 5 MHz.

The logic unit of the counter is contained in a QuickLogic FPGA chip. The normal procedure to start the synchronisation process is to use one second as the initial measurement time, giving a coarse adjustment of the oscillator frequency. The next step is to increase the measurement time and make finer adjustments until the stability limit of the oscillator is reached.

The stability of the oscillator within one day ($5x10^{-10}$), corresponds to 1 period of 50 MHz in 40 seconds.



Figur3 *Basic structure of the GPS synchronisation unit*

The main purpose of the clock is to make it possible to have synchronised time at separate measurement sites with high accuracy. However, the design of the unit is so versatile that it can be used for various other applications. A possible use is for frequency measurements or measurements of time delays.

The unit is also equipped with a digital direct synthesis chip (DDS). This chip can produce a sinusoidal signal with precisely controlled frequency, phase and amplitude. The output frequency can be set to any frequency from DC to 50 MHz with a resolution of about 1/100 Hz . The unit also has a microphone input. With this, the DDS signal can be modulated in frequency, phase or amplitude in real time.

2.2 PCB

The PCB is a two layer board, 260x200 mm large, as shown in figure 4.

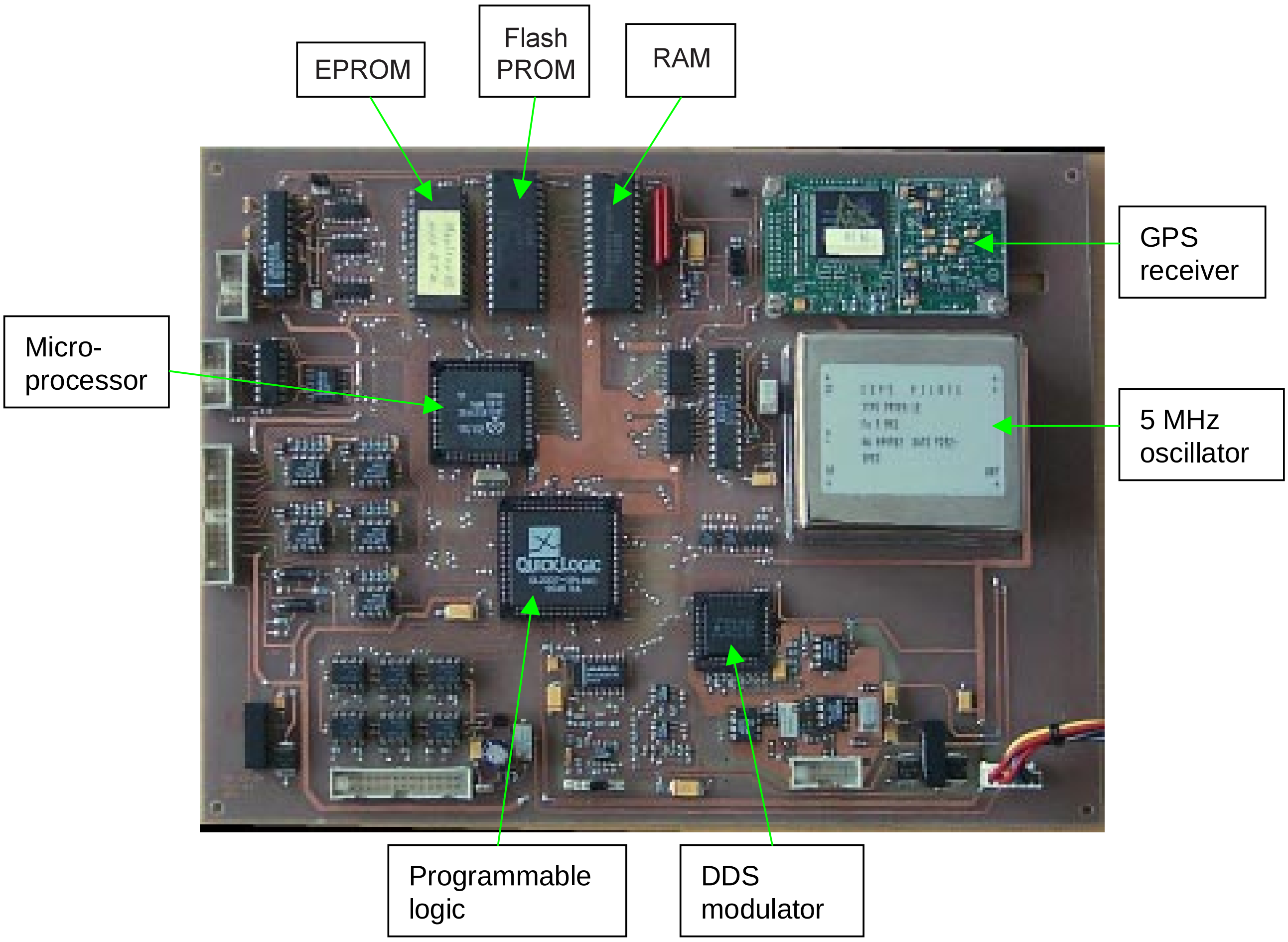


Figure 4 *The PCB.*

2.3 Main components

2.3.1 Oscillator

The oscillator, a PMTP 5.1E, with a frequency of 5 MHz is manufactured by CEPE (Compagnie d´électronique et de piézo-électricité). It is a crystal oscillator operated in a capsule with regulated temperature, enclosed in a small sealed metal package. It has a short term stability (up to 10 seconds) of 10^{-12}. The one day stability is $5x10^{-10}$ and the one month stability is 10^{-8}(reference 3).

2.3.2 GPS receiver

The GPS receiver is of the type Rockwell TU30-D140 "Jupiter". It is a 12 parallel-channel receiver. It can accept Differential GPS (DGPS) corrections in the RTCM SC-104 format. Its size is 71 x 41 x 11 mm (reference 2).

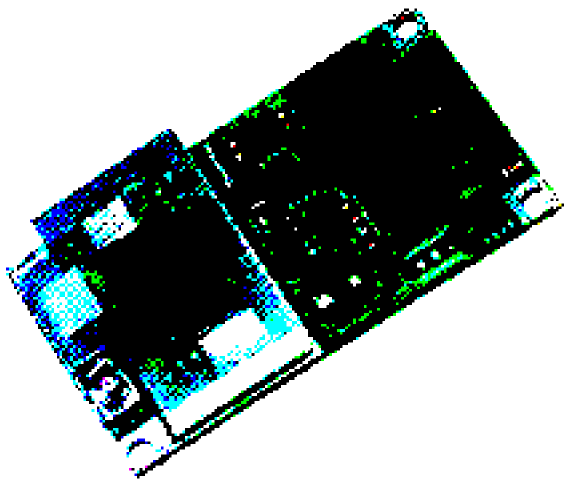


Figure 5 *The GPS receiver*

2.3.3 Microprocessor

The microprocessor is a Hitachi HD64180 eight-bit processor. It is connected to three different memory chips – a 16 kB EPROM, a 16 kB Flashprom and a 32 kB RAM chip.

2.3.4 Direct Digital Synthesis chip

This is a AD7008 CMOS DDS Modulator manufactured by Analog Devices. This chip can generate sinusoidal signals with frequencies from DC up to 50 MHz in steps of about 1/100 Hz (50000000 / 2^{32}) and with the same stability as the 5 MHz oscillator. The signal can be modulated in amplitude, frequency and phase. The speed of the modulation is only limited by the microprocessor (figure 6 and reference 4).

2.3.5 Quick-Logic programmable logic

Most of the logic for counters and time-keeping is programmed in a Quick-Logic programmable chip, QL2007 (5). This means that it is easy to change the behaviour of the clock and to add new functions without having to change the main PC-board.

2.4 Software

The EPROM contains a monitor program with debugging tools, flash memory programming routines, a routine for loading program from a host, and a real time kernel. The kernel handles the time scheduling of several concurrently running tasks. The executable code of the tasks is stored in the flash PROM or RAM.

The real-time tasks interprete the GPS receiver messages and the host commands, and handle the GPS synchronisation.

In the normal use of the clock a simple command language is used. It includes commands to control the timing of the output pulses, the pulse lengths and the signal waveforms.

With the aid of a Windows based Fortran program the user can set parameters to control the pulse shapes and timing, as well as display the GPS position, and perform frequency and time measurements.

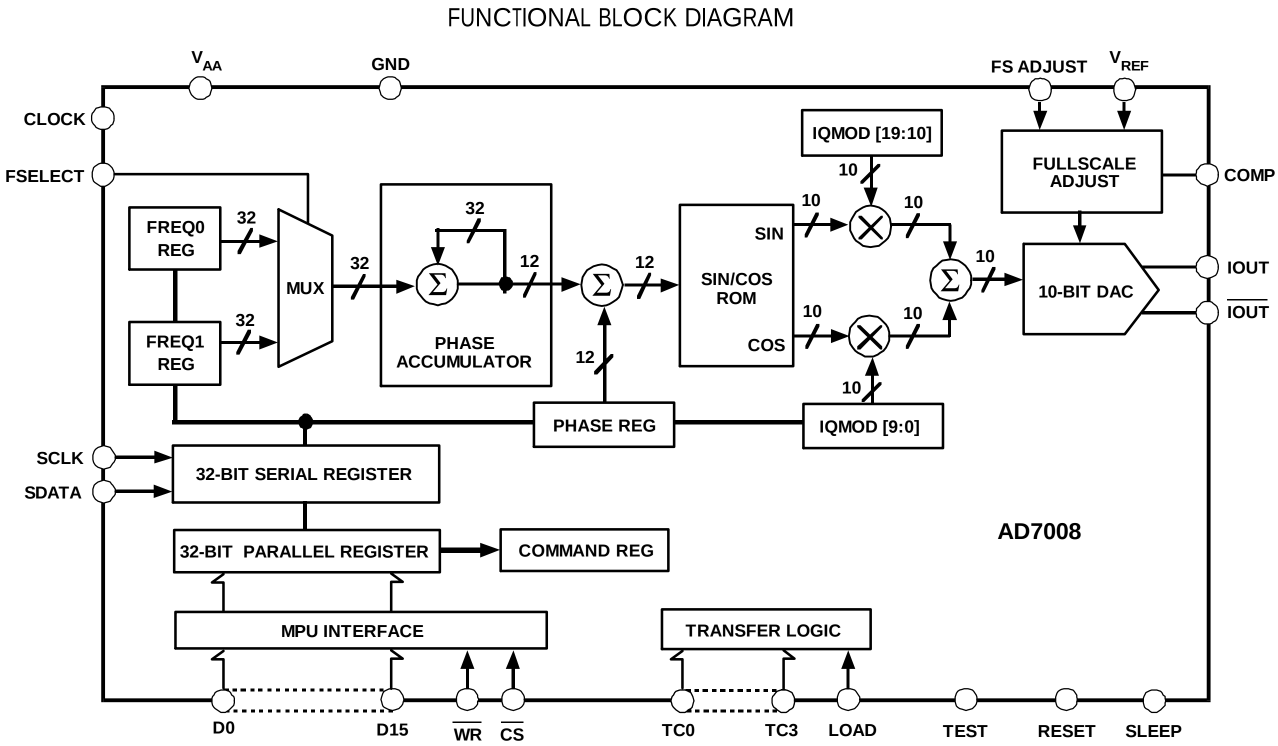


Figure 6. *The DDS Functional Block Diagram*

3. First test results

Figures 7 - 9 show the behaviour of the clock during the first minutes after power on. The blue curve shows the difference between the output frequency of the clock measured between two consecutive GPS one-second-pulses and 50 MHz. The negative spikes in the curve are due to a counter being reset at regular intervals. You should only look at the positive envelope of the curve. The green curve is the control signal to the D/A-converter that steers the oscillator frequency. We can se three distinct phases of the control loop. During the first few seconds the D/A output is steered in very coarse steps to find a value where the frequency drift of the oscillator is towards 50 MHz. Then, in the second phase, the D/A converter is left in that state and the difference

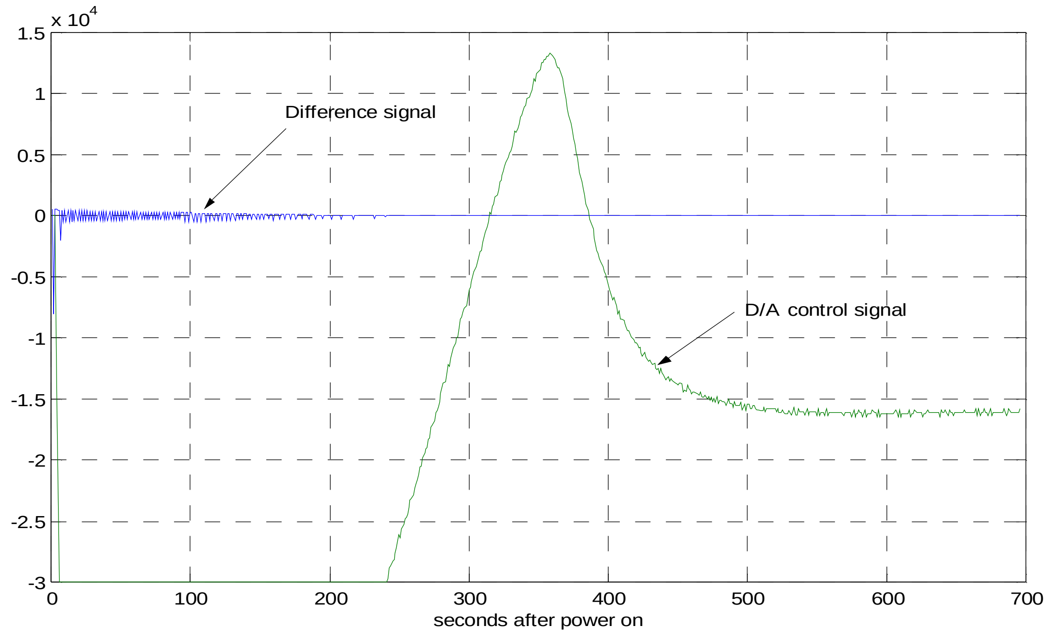


Figure 7. *Power on behaviour of GPS synchronised clock. The green curve is the D/A control signal and the blue curve the deviation from 50 MHz. The vertical scale for the difference signal is in Hz. The D/A control signal has an allowed interval of ±32767.*

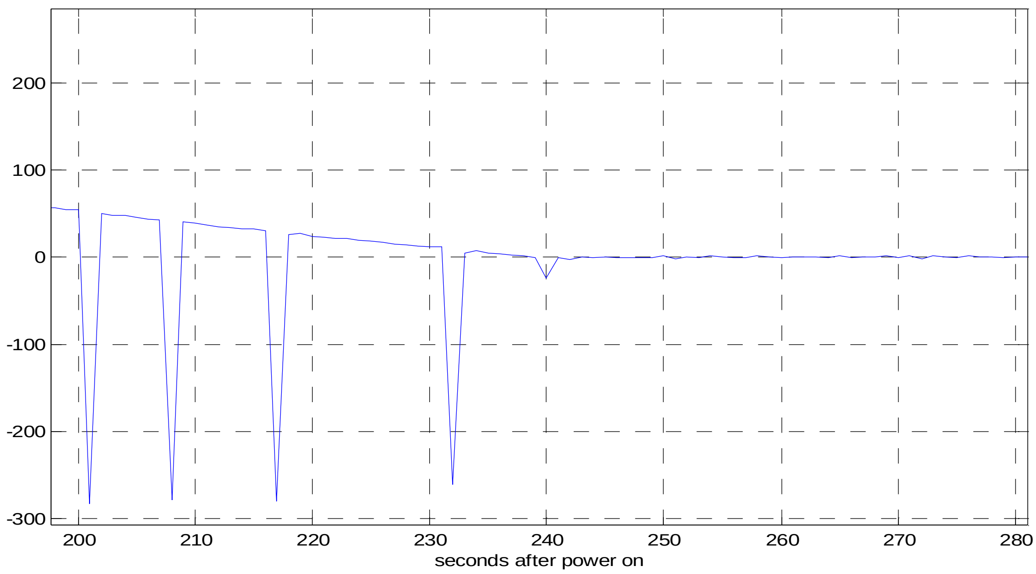


Figure 8. *Close up of the beginning of phase three in the control loop.*

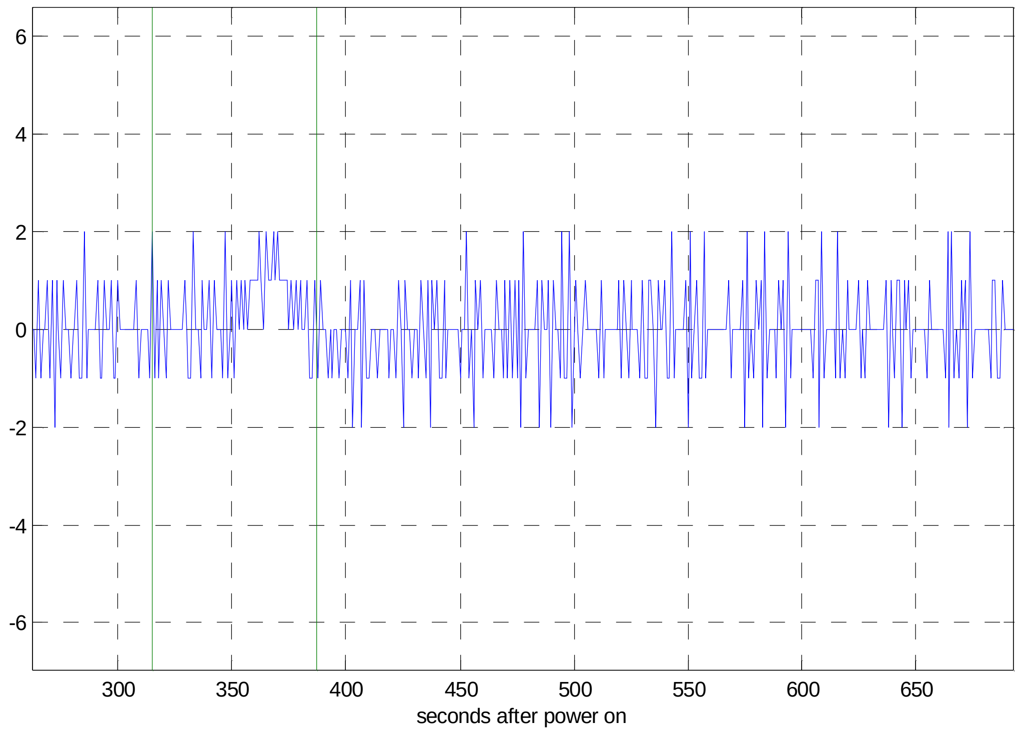


Figure 9. *Close up of the second half of the power up sequence.*

(blue curve) is monitored. After 241 seconds when the frequency just reaches 50 MHz the third phase of the control loop begins. The stability of the oscillator is now so good so that it is worth controlling it with the D/A-converter. As can be seen from the blue curve, the behaviour of the control loop is excellent. The mean absolute difference is only 0.65 periods corresponding to 13 nanoseconds from 250 seconds after power on to the end of the curve. After about 600 seconds the D/A output has stabilised indicating that the oscillator oven has reached its final temperature. At this point the next phase in the control loop should start with difference measurements over successively longer periods and more fine-tuning of the oscillator. That part of the program however is not yet written.

4. Conclusion

Preliminary tests of the systems indicate that the accuracy of the synchronised clock far exceeds our requirements. Further work is needed to verify the long-term stability. We also need to build a second clock unit to make a complete system for multistatic sonar.

5. References

1. L. Mozzone: ”Deployable multistatic active sonar: the cycle of system design, tests and data analysis”, Oceans’ 98 conference, Nice, France September 1998.
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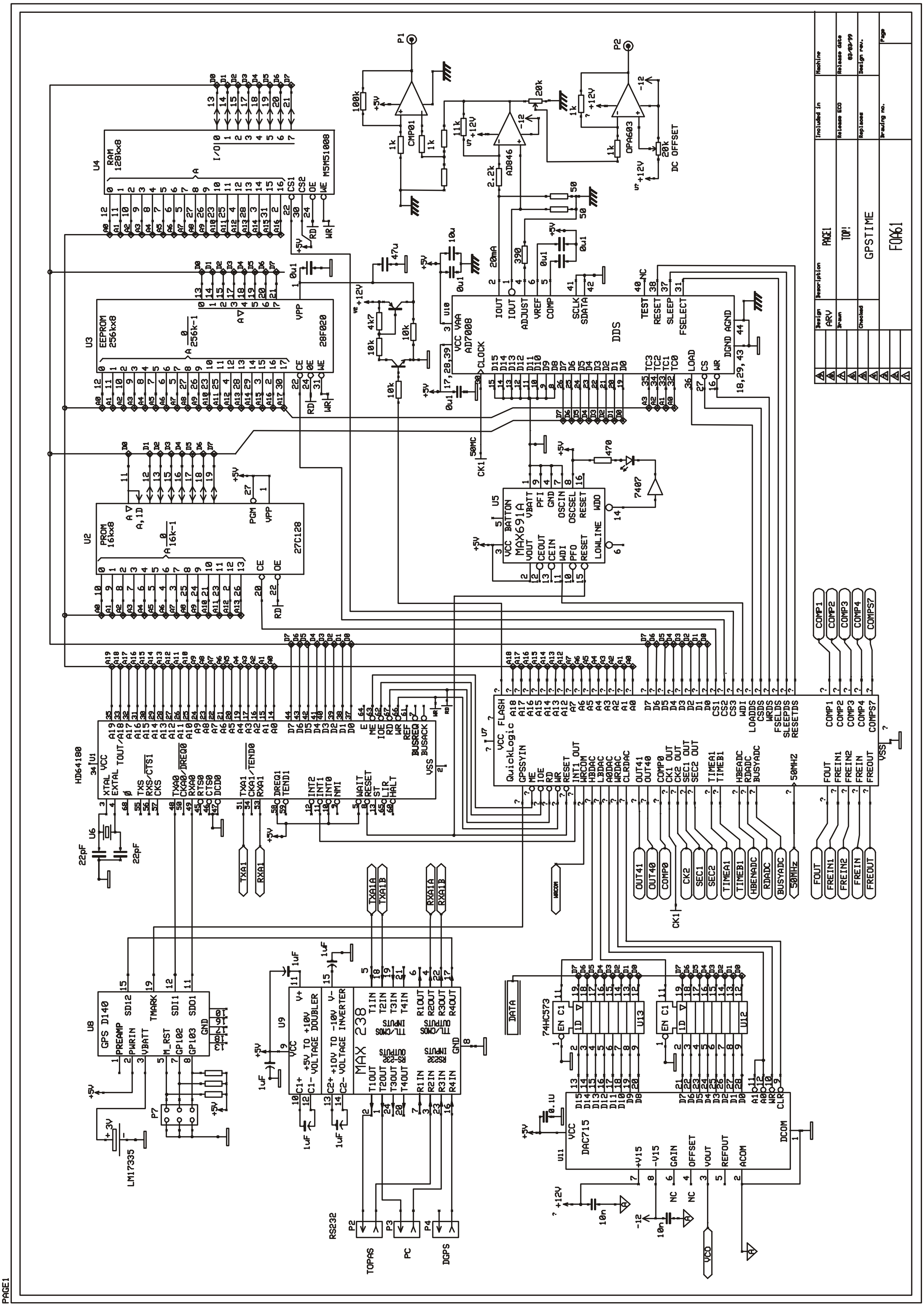
4. Analog Devices, CMOS DDS Modulator AD7008 Rev B. C1791a-10-2/95. Data sheet 1995.
5. Quick Works Users Guide ver. 7.0, 1991-1998.

Appendix A
Design of the electrical circuit

Contents A-1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DDS
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GPS D140
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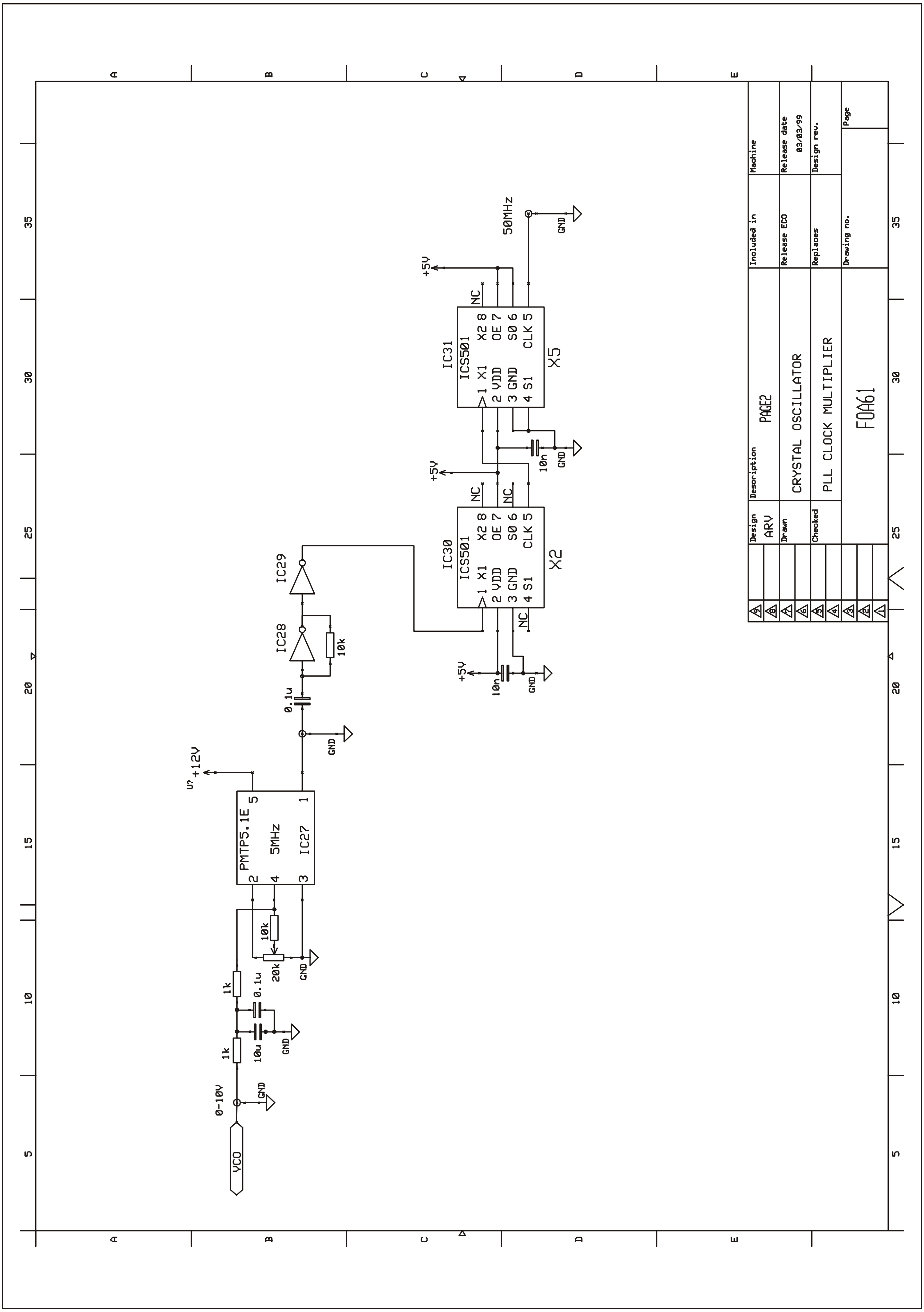

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1k
20k
10k
PMTP5.1E
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0.1u
IC28
10k
IC29
IC30
ICS501
1 X1
2 VDD
3 GND
4 S1
X2 8
OE 7
S0 6
CLK 5
X2
NC
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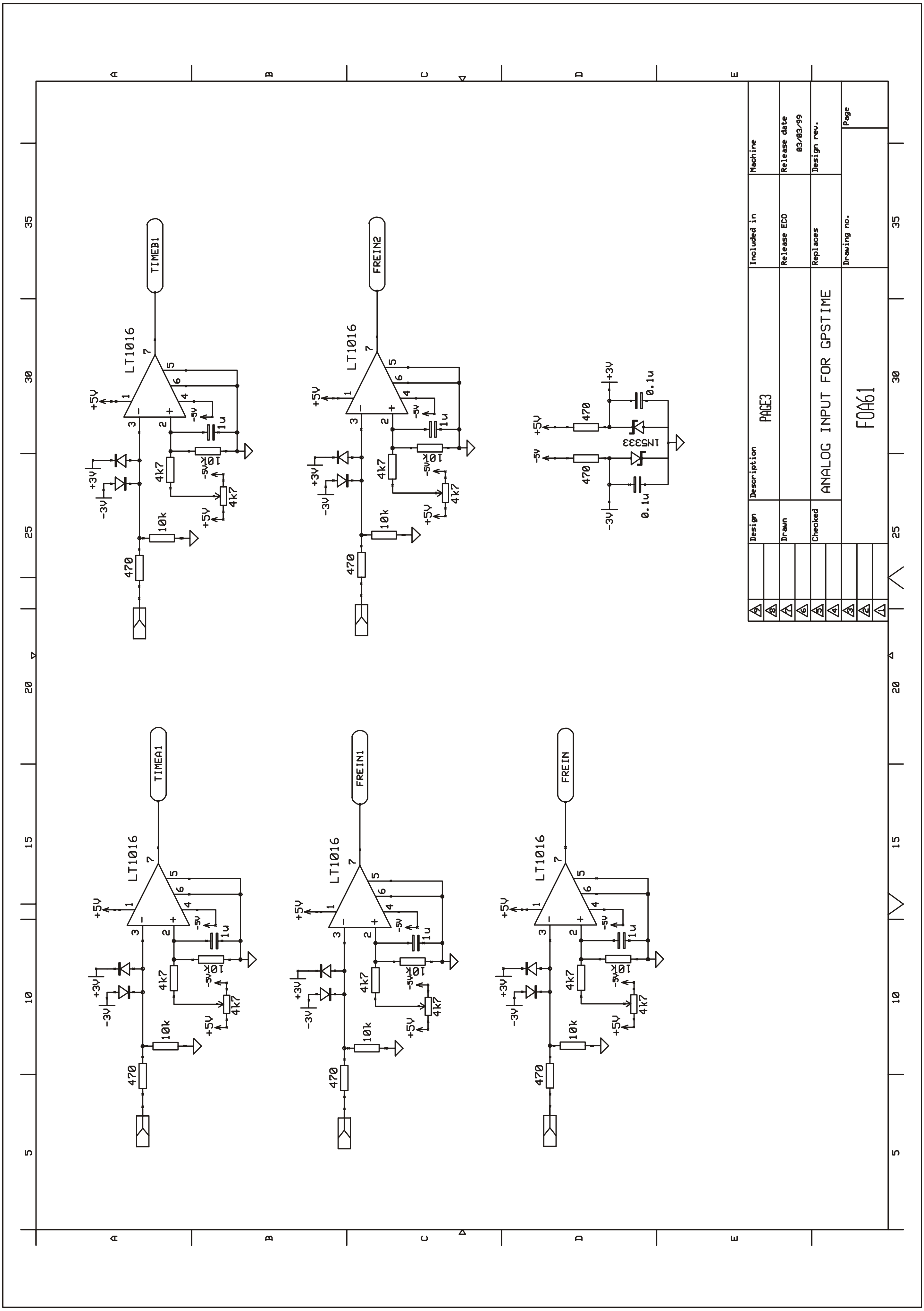

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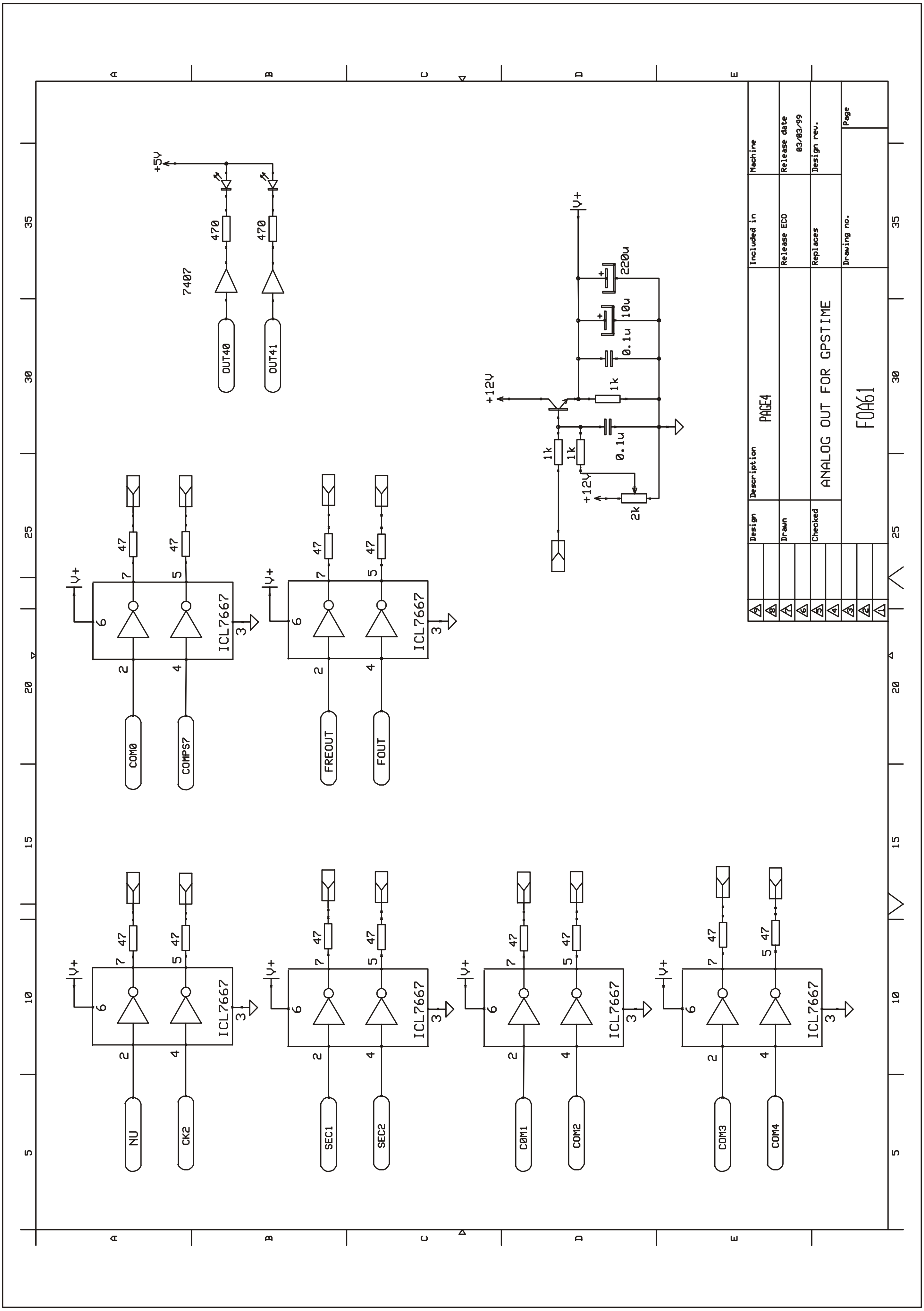
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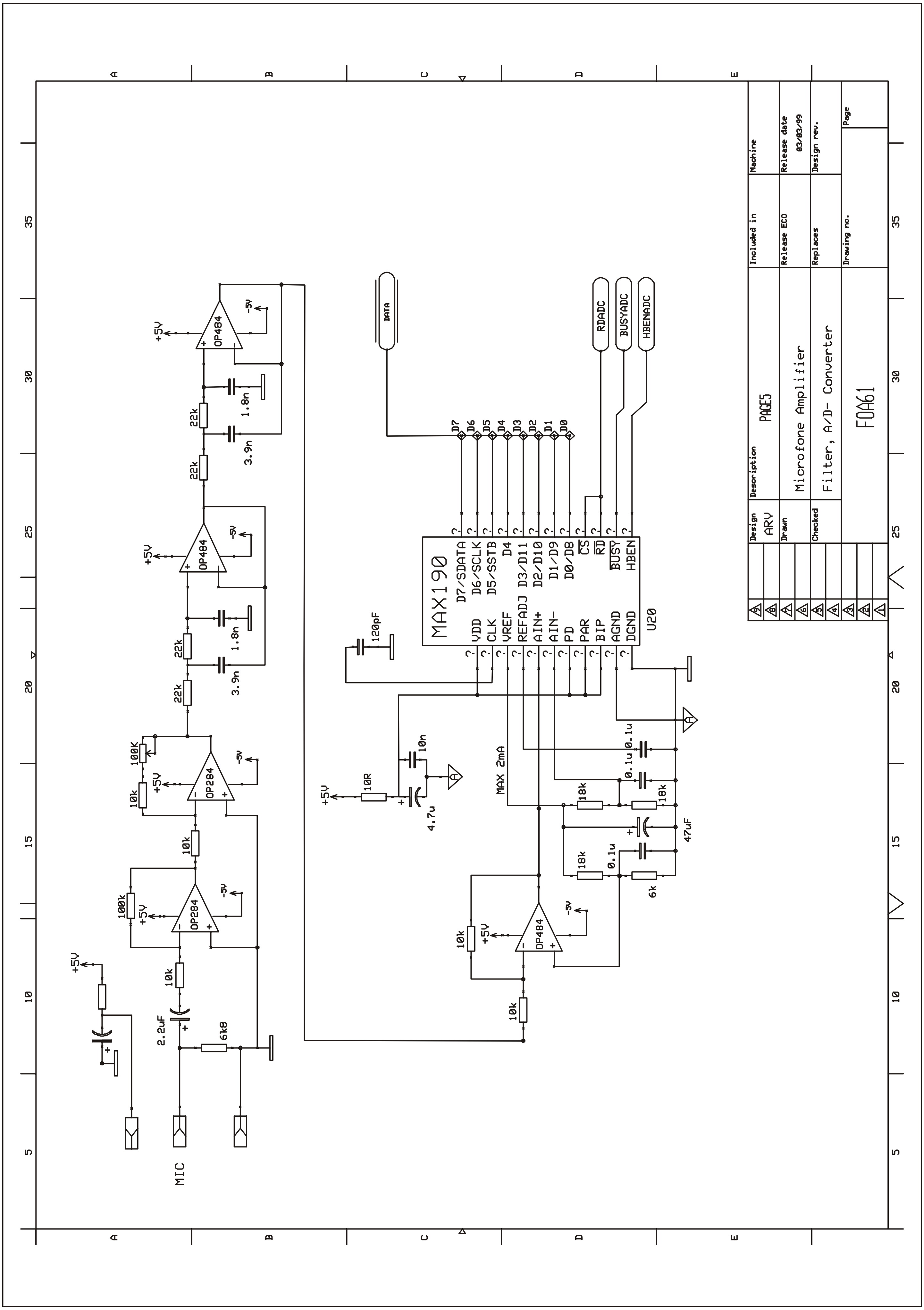
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RD
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VDD
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PAR
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AGND
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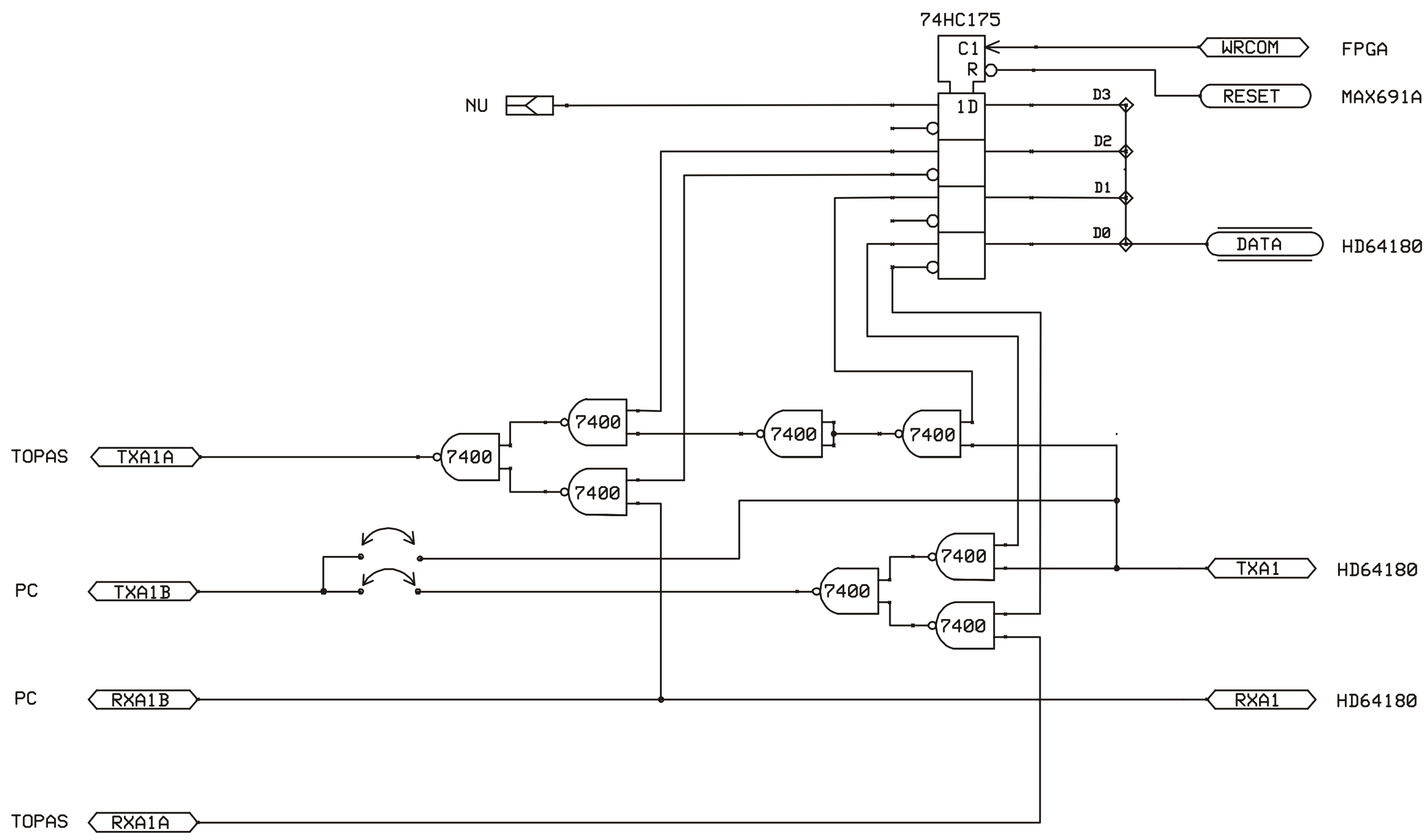

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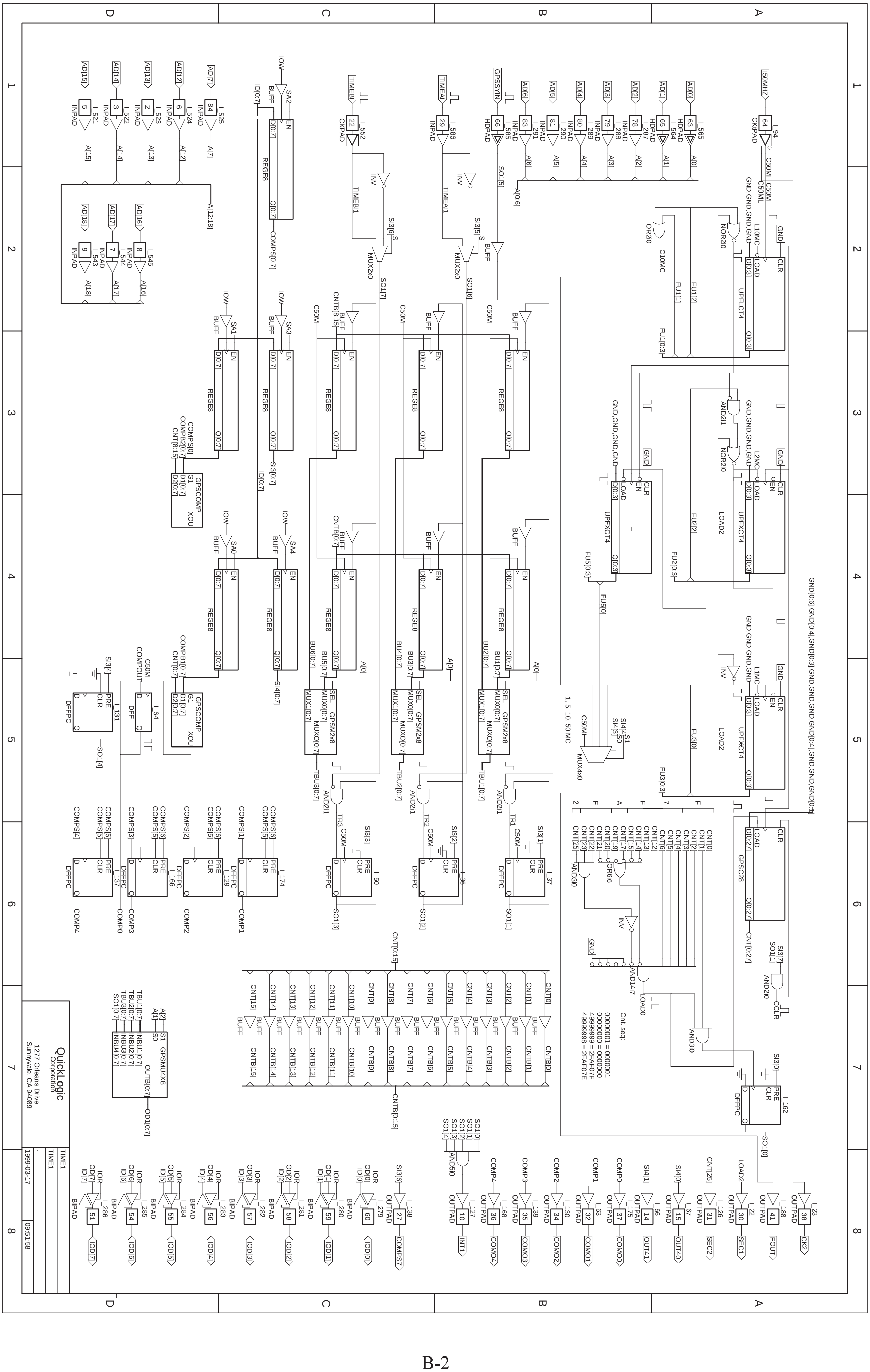
Appendix B

Quick logic circuit diagrams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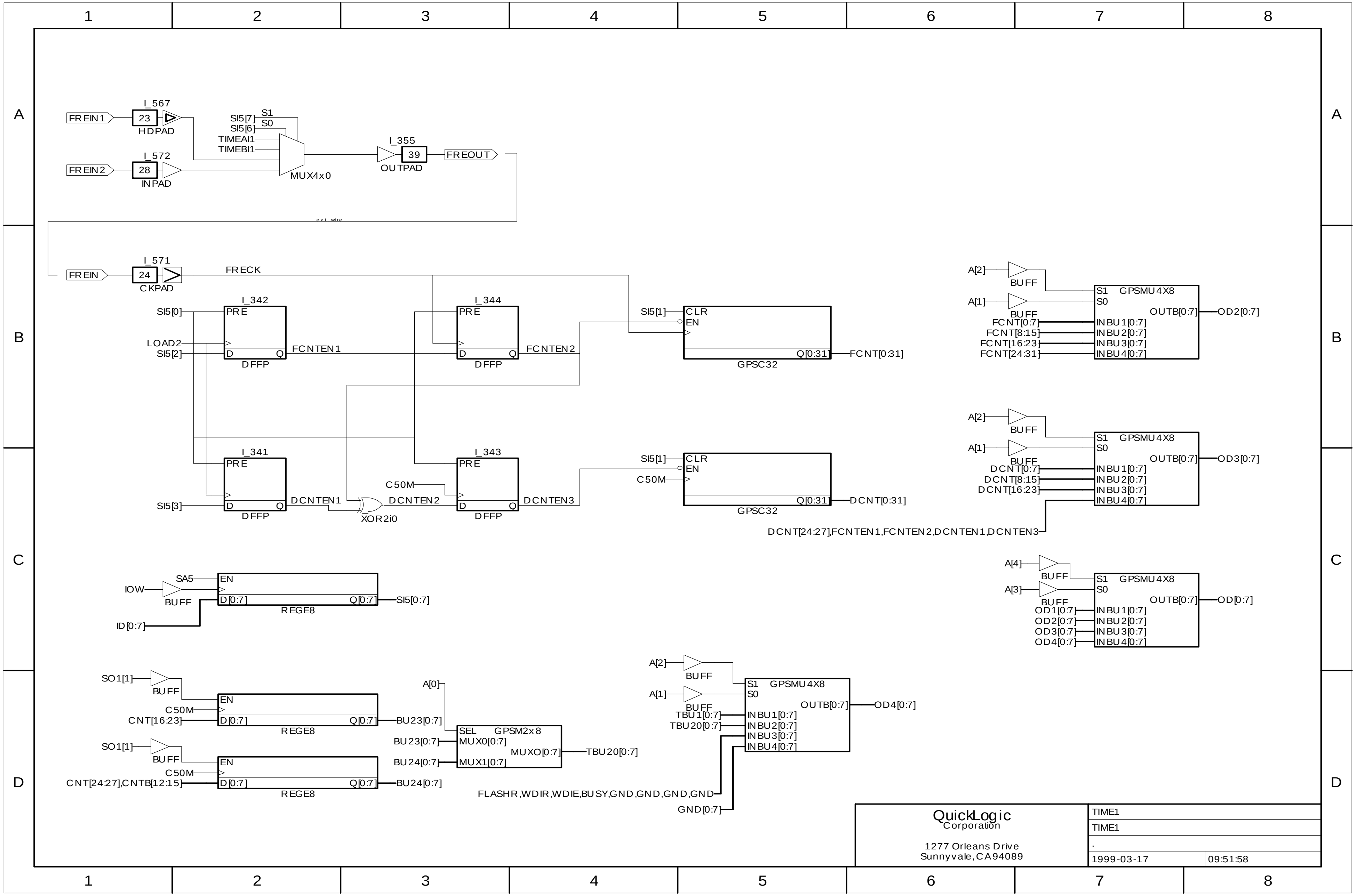
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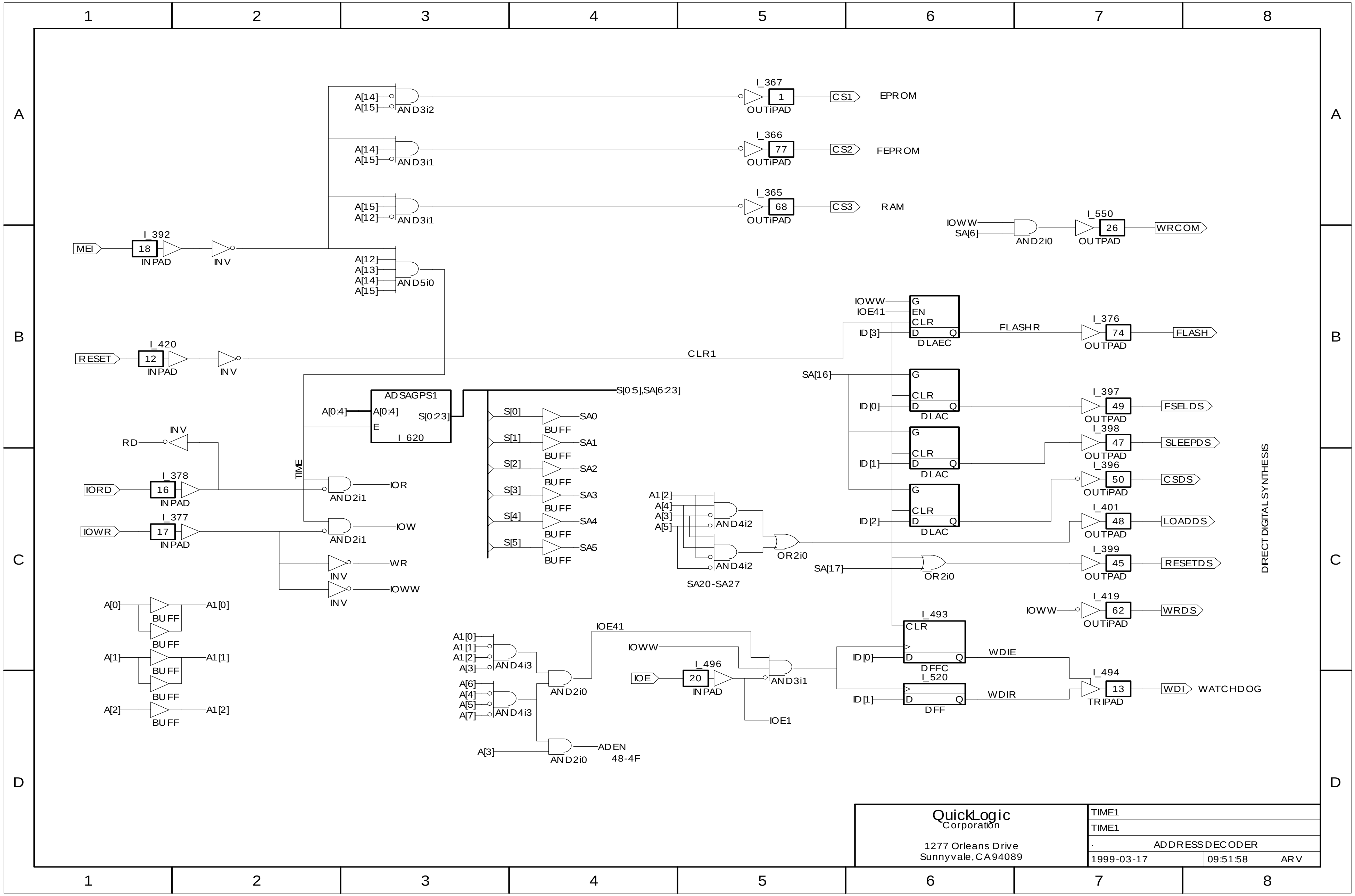

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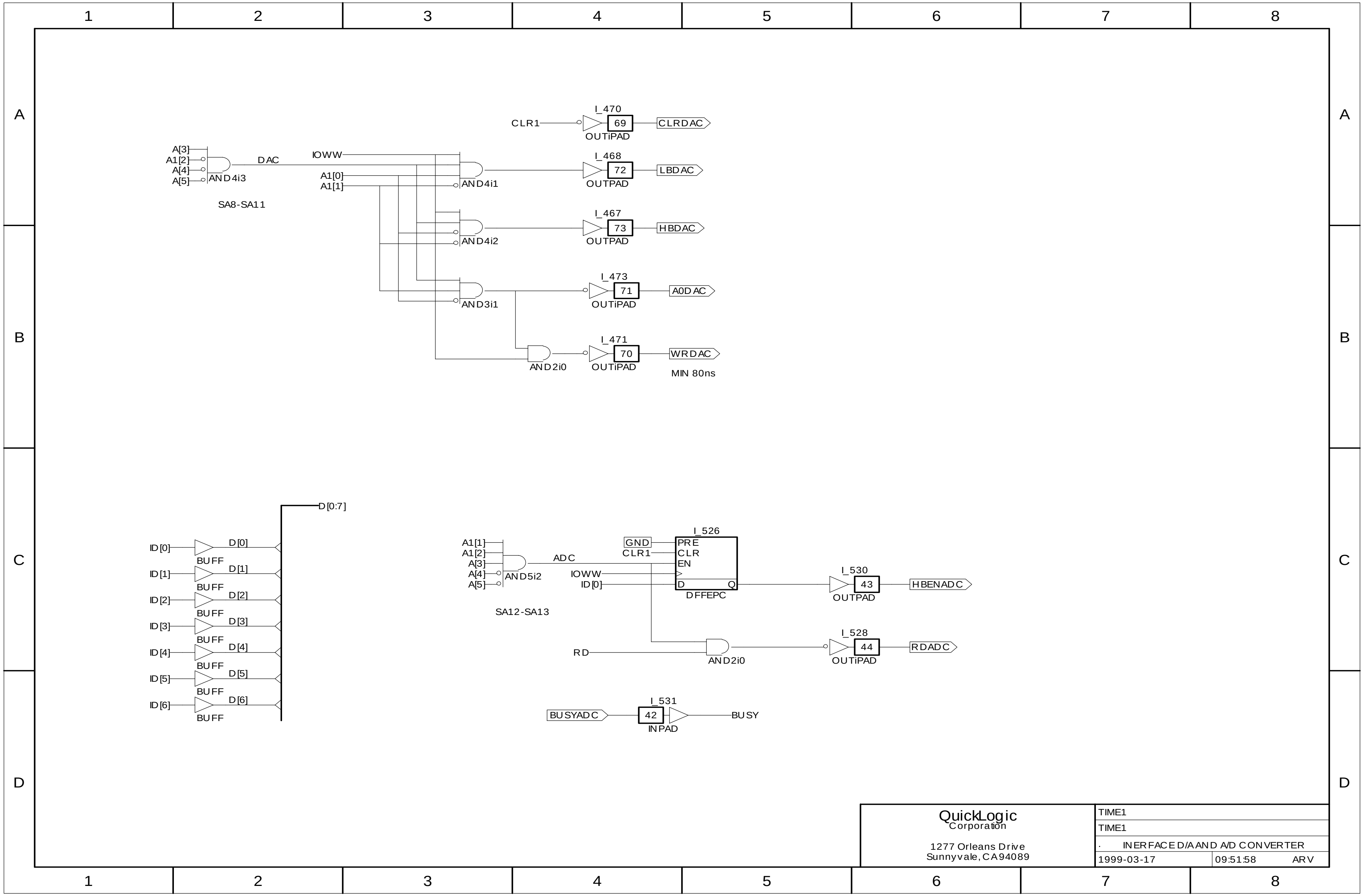
09:51:58
ARV



1 2 3 4 5 6 7 8
A B C D
I_470
CLR1
69
CLRDAC
OUTiPAD
A[3]
A1[2]
A[4]
A[5]
AND4i3
DAC
IOWW
A1[0]
A1[1]
AND4i1
I_468
72
LBDAC
OUTPAD
SA8-SA11
I_467
73
HBDAC
OUTPAD
AND4i2
I_473
71
A0DAC
OUTiPAD
AND3i1
I_471
70
WRDAC
AND2i0
OUTiPAD
MIN 80ns
D[0:7]
ID[0]
D[0]
BUFF
ID[1]
D[1]
ID[2]
D[2]
ID[3]
D[3]
ID[4]
D[4]
ID[5]
D[5]
ID[6]
D[6]
A1[1]
A1[2]
A[3]
A[4]
A[5]
AND5i2
ADC
SA12-SA13
GND
CLR1
IOWW
ID[0]
I_526
PRE
CLR
EN
D
Q
DFFEPC
I_530
43
HBENADC
OUTPAD
RD
AND2i0
I_528
44
RDADC
OUTiPAD
BUSYADC
I_531
42
INPAD
BUSY
QuickLogic
Corporation
1277 Orleans Drive
Sunnyvale, CA 94089
TIME1
TIME1
INERFACE D/A AND A/D CONVERTER
1999-03-17
09:51:58
ARV

Appendix C

Description of I/O ports

Analogue inputs

Time A Used for start signal in Time A – Time B measurement

Time B Used for stop signal in Time A – Time B measurement

Frequency in 1 Input for frequency measurements

Frequency in 2 Input for frequency measurements

Frequency in Input for frequency measurements

GPS antenna Input from the active GPS antenna

Microphone input Input for condenser microphone. Low pass filtered at 3.3 kHz. Maximum sampling frequency 70 kHz.

All inputs have BNC-connectors, except the GPS antenna which has a TNC-connector and the microphone input which has an 3.5 mm earphone connector

Analogue outputs

50 MHz 50 MHz square wave

1 second pulse Short pulse

1 second pulse Long pulse

Com1 – Com4 These are four outputs on which can be generated pulses at arbitrary predefined time points.

Com0 On this output is generated a pulse at the same time as the pulse at one of the outputs Com1 – Com4.

Freout To this output is multiplexed one of the inputs Frequency1, Frequency2, TimeA or TimeB.

Fout This output can be programmed to give 1, 5 , 10 or 50 MHz square wave.

DDS out 1 Linear (sine wave) output from DDS chip.

DDS out 2 Square wave output from DDS chip.

All these outputs have BNC-connectors. The level of the outputs can be chosen within 3 - 12 V.

Serial I/O

There are three 9-pin Dsub connectors.

DGPS Input for differential GPS message. Unidirectional.

PC For communication with PC host.

Sonar This connector is for communication with the sonar transmitter that we are going to use in the bistatic experiments.

The connections between PC, sonar and the microprocessor are controlled by the microprocessor. There is no direct path to the GPS receiver, which is accessed via the microprocessor.

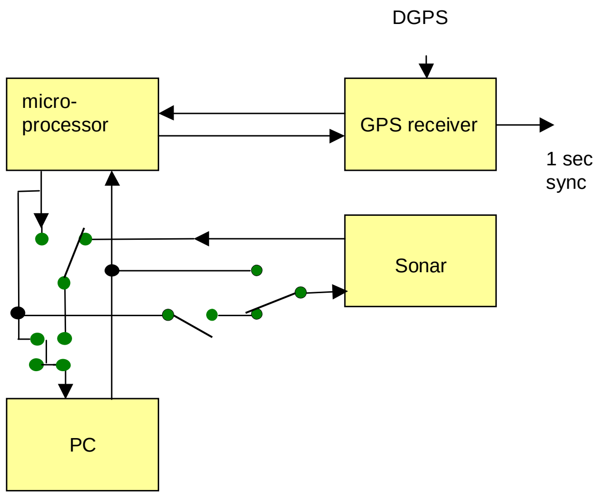


Figure 2.4 *The RS232 connections*

Power input

220 V AC

12 V DC

LED

The front panel of the clock has three LEDs that can be programmed to show status.